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(54) Ball grid array package for an integated circuit and method of reducing ground bounce

Packung mit Lötballgitter für eine integrierte Schaltung

Boîtier à réseau de billes pour circuit intégré

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Description

[0001] The invention relates to a ball grid array package according to the preamble of claim 1 and to a method of reducing ground bounce according to the preamble of claim 13.

[0002] This invention thus relates to packaging integrated circuits, and more particularly to improving thermal and electrical characteristics in ball grid array packaging for high speed integrated circuits.

[0003] Integrated circuits ("ICs") are fabricated on a semiconductor substrate that is mounted within a typically epoxy or ceramic overmold for later mounting on a printed circuit board ("PCB"). As fabrication techniques improve, ICs tend to include circuits with increased complexity and increased number of input and output leads ("pinouts"). Further, as more transistors are fabricated on an IC die of a given size, dissipating heat from the IC becomes a greater challenge.

[0004] One packaging system for providing an IC with a large number of pinouts in a relatively small package area is known as the ball grid array ("BGA") package. Figure 1 depicts a standard two-layer BGA mounting system, similar to the so-called OMNI™ system promoted by Motorola, Inc. In this system, a BGA package 2 includes a double-sided copper clad printed circuit board ("PCB") 4 with conductive and/or thermal vias 6A, 6B, 6C connecting upper BGA package conductive traces 8A, 8B, 8C to lower BGA package conductive traces 10A, 10B, 10C. The 8A traces and the 8B traces may each be donut-shaped, as may the corresponding 10A and 10B traces. The various vias preferably are identical and may be referred to interchangeably as conductive or thermal vias.

[0005] The BGA package further includes the IC die 12 to be packaged, and a plurality of meltable solder balls 14A, 14B, 14C in contact with the lower conductive traces 10A, 10B, 10C. The upper and lower BGA package traces 8A, 8B, 8C, 10A, 10B, 10C are typically formed by etching the copper clad upper and lower surfaces of BGA PCB 4. An overmold, shown in phantom as 16, encapsulates and thus protects the IC die 12. Overmold 16 could, of course, be sized to extend over a greater or lesser portion of the upper surface of BGA package 2 than what is depicted in Figure 1.

[0006] Package 2 will eventually be soldered to a system printed circuit board ("PCB") 18, whose upper surface includes conductive traces 20A, 20B, 20C that will contact various of the solder balls 14A, 14B, 14C. Thus, while Figure 1 shows BGA package 2 and system PCB 18 spaced apart vertically, in practice the solder balls and the system PCB traces are placed in contact with one another, whereupon an infrared reflow process melts the solder balls. Upon melting, the solder balls electrically and mechanically join various of the BGA package traces 10A, 10B, 10C to various of the system PCB traces 20A, 20B, 20C. The various solder balls may be arrayed in a relatively dense matrix, with adjacent balls being spaced-apart horizontally 0.050" to 0.060" (1.3 mm to 1.5 mm). As a result, BGA package 2 can advantageously provide a dense pattern of pinout connections with IC 12.

[0007] Those skilled in the art will appreciate that IC 12 may include various semiconductor devices such as bipolar or metal- oxide-semiconductor ("MOS") transistors, as well as effective resistor and capacitor components. These transistors and components will form one or more circuits that are typically coupled to an upper power source Vdd, and to a lower power source Vss (usually ground).

[0008] Bonding wires such as 22, 24 make electrical connection from pads formed on IC 12 (not shown) to a BGA package trace or plane formed by etching the copper clad on the upper surface of BGA structure 2. Bond wire 22, for example, connects to a BGA package Vdd upper plane trace 8A that connects to a conductive via 6A, which connects to a BGA package Vdd lower plane trace 10A that connects to a solder ball 14A. On the underlying system PCB 18, one or more system PCB traces 20A couple to the Vdd power source that is connected to the system PCB 18. In similar fashion, one or more bond wires (not shown) will couple IC 12 to Vss on the system PCB 18.

[0009] Similarly, bonding wire 24 is shown coupled to an upper signal BGA package trace 8B that is connected to vias 6B, to BGA package lower signal trace 10B, and signal solder balls 14B. On system PCB 18, system PCB traces 20B couple electrical signals to or from IC 12. Other bonding wires will also be present but are not shown for ease of illustration. Of course, IC 12 will generally be coupled by various bond wires, upper BGA package traces, vias, lower BGA package traces to various different signal solder balls, for contact with various system PCB 18 signal traces.

[0010] As shown in Figure 1, the lower substrate surface of IC 12 is connected to a BGA package IC die Vss plane 8C, that connects through several vias 6C to a BGA package lower surface Vss plane 10C to which solder balls 14C are attached. As noted, Vss connections to IC 12 generally are also brought out through Vss IC pads, bond wires, traces, vias, traces and solder balls in a manner similar to what is described herein with respect to the connections for Vdd. The underlying system PCB 18 includes a system PCB Vss ground plane 20C that electrically connects to such Vss solder balls, including solder balls 14C.

[0011] BGA package 2 is relatively economical to manufacture because PCB 4 may be a symmetrical and relatively inexpensive generic commodity. By symmetrical, it is meant that PCB 4 is manufactured with copper clad on the upper and lower surfaces of a typically epoxy glass core 22, commonly referred to as FR4 material. (It is from this copper clad that the upper and lower BGA package traces or planes 8A, 8B, 8C, 10A, 10B, 10C are formed.) Alternatively, core 22 may be fabricated from an adhesive-like resin commonly termed pre-preg.

[0012] It is important that PCB 4 be sufficiently rigid so that the various solder balls will register properly for soldering to corresponding system PCB traces. As a result, the vertical thickness of core 22 in Figure 1 will typically be at least 0.02" to 0.03" (0.5 mm to 0.8 mm).

[0013] Although the BGA configuration of Figure 1 has the advantage of being inexpensive to fabricate, it has several shortcomings. Specifically, BGA 4 does not provide a good signal plane for current surges into or out of IC 12, and does not do a good job of dissipating heat generated by IC 12. The relatively poor electrical and thermal performance associated with BGA structure 4 is especially apparent when IC 12 includes high density, high frequency digital circuitry. Essentially these performance shortcomings arise because the efficient system Vss and Vdd planes on PCB 18 are too far away from IC 12 to be truly effective.

[0014] Thermally, although the system PCB Vss plane 20C can sink heat dissipated by IC 12 and downconducted through vias 6C, the system PCB Vss plane is just too remote for good dissipation. The prior art configuration of Figure 1 has a thermal resistance θ_{ja} of about 35°C/W, which means that for an increase of one watt dissipation, the junction temperature of the IC die 12 will increase 35°C. As a result, IC 12 may overheat, or require bulky and relatively expensive heat sinking. Alternatively, IC 12 may have to be operated at a lower equivalent duty cycle to reduce dissipation, thus sacrificing IC 12 performance because of the poor thermal characteristics associated with prior art two-layer BGA packages.

[0015] Electrically, the current paths from the system PCB Vdd plane 20A, up into IC 12, through the system Vss plane 20C, and vice versa, are simply too long. As will be described, these long path lengths can result in the Vdd and Vss potentials within IC 12 impermissibly varying in magnitude during current surges. What occurs is that an effective inductance L exists in series with the relatively long power supply current paths. Large mutual inductances may be present that force some transient surge ground current to return undesirably through IC 12, rather than through the system PCB planes. This IC 12 transient surge current flow can cause ground bounce and crosstalk between various circuits within IC 12. In addition, the effective inductance L can contribute to an undesirable time delay for signals propagating through IC 12.

[0016] More specifically, an excessively long path between a signal node on the IC chip and a signal return ground plane increases the effective series inductance (L) therebetween. In the presence of current spikes through such path, the voltage at the Vss pad(s) and/or Vdd pad(s) within IC 12 can deviate or "bounce" from their nominal DC voltage.

[0017] Consider, for example, the effect of a relatively long current return path for a high speed CMOS digital circuit fabricated within IC 12. The output of circuit typically will include a PMOS pull-up and an NMOS pull-down transistor coupled in series between Vdd and Vss. When outputting a digital "1", the NMOS transistor is off, and the PMOS transistor is on, and the circuit sources current from Vdd through the PMOS transistor to an output load coupled to Vss. When outputting a digital "0", the PMOS transistor is off, the NMOS transistor is on and sinks current from the output load.

[0018] But when this CMOS circuit changes states from "1" to "0" or vice versa, for a brief interval the PMOS and NMOS transistors may both be simultaneously on due to imperfect switching. When both transistors are on during transitions a rapid change (or "spike") in current (di/dt) through the circuit can occur. In the presence of series inductance L, current spiking results in an L di/dt = dV/dt change or "bounce" in the voltage present at the Vdd and/or Vss pads on IC 12. Ground bounce results from this dV/dt for Vdd and/or Vss within IC 12.

[0019] Such voltage bouncing within IC 12 is especially troublesome at "0" to "1" transitions because CMOS transistors exhibit less noise immunity margin for error near "0" voltage states as contrasted to "1" voltage states. For this reason, it is especially important that a low inductance impedance Vss path within IC 12 be maintained.

[0020] In addition to producing overshoot and undershoot on output voltage waveforms, ground bounce can degrade digital switching reliability. This degradation occurs because any variations in Vdd or Vss within IC 12 can alter CMOS trip points.

[0021] Generally, the configuration of Figure 1 will exhibit an output impedance between a signal output pad on IC 12 and Vss of about 250 Ω. A 250 Ω output impedance is undesirably high for matching to a system PCB that typically is characterized by an impedance in the 50 Ω to 75 Ω range. The resultant impedance mismatch contributes to overshoot and ringing on signals coupled from the BGA package to the system PCB. The configuration of Figure 1 also exhibits an effective series inductance of 12 nh to 15 nh, and an equivalent output shunt capacitance at a signal output pad of about 1.2 pF.

[0022] As noted, the series inductance can produce overshoot and ringing in IC 12 signals, especially when a relatively light capacitive load is to be driven. Further, the series inductance and shunt capacitance associated with the two-layer BGA package of Figure 1 can undesirably delay a signal passing through IC 12 by several nanoseconds. If IC 12 includes high speed switching devices (e.g., wherein the operating frequency is greater than 30 MHz), a BGA package-imposed time delay of a few nanoseconds may be unacceptable.

[0023] In summary, there is a need for a BGA package having improved thermal and electrical characteristics, especially for high speed digital ICs. To reduce ground bounce and enhance IC operating reliability, such BGA package should preferably exhibit approximately 50Ω output impedance and decreased effective series inductance. Further, it should preferably be possible to manufacture such a BGA package using generic symmetri-

cal PCB materials.

[0024] Known from US-A-4 739 448 is a ball grid array package for an integrated circuit comprising upper and lower layer package traces, a plurality of vertically arranged layers comprising a signal line layer, a ground layer, a power conductor layer and separating layers in between, and a plurality of vias each extending between and soldered to opposing surfaces of adjacent layers.

[0025] The invention is defined in claims 1 and 13.

[0026] In a first three-layer embodiment, the present invention provides a BGA package with a BGA Vss plane disposed between the upper and lower BGA package traces. Further, this embodiment also provides upper and lower BGA package Vss traces on the outer periphery of the BGA package, to help maintain a low impedance between an IC packaged with the three-layer embodiment, and the BGA Vss plane. This embodiment is three-layered in that there are traces at the upper surface of the BGA package, there is an inter-mediate BGA Vss plane, and there are traces at the lower surface of the BGA package.

[0027] The additional BGA Vss plane preferably is a copper clad surface on a portion of PCB material from which the BGA package is fabricated. IC-generated heat is coupled from the BGA package IC die Vss trace through vias to the BGA Vss plane, through the lower portion of the same vias to the BGA package Vss trace on the lower surface of BGA package, as well as to a Vss plane on the underlying system PCB. The BGA Vss plane is closer to the IC than is the underlying system PCB, and thus performs an IC heat sinking function by lowering thermal resistance θ_{ja}.

[0028] The BGA Vss plane also provides a closer Vss plane for sinking current output by the IC than is provided by the underlying PCB Vss plane. The presence of this closer Vss plane reduces series inductance to the IC, reduces ground bounce, at least for IC output signals transitioning from "1" to "0", and reduces time delay through the IC. While the closer Vss plane reduces series inductance, closer Vss plane proximity to the IC slightly increases shunt capacitance as seen by a BGA package upper surface trace to Vss. However, the slight increase in shunt capacitance appears beneficial in reducing noise seen by the IC.

[0029] A more preferred embodiment of the present invention provides a four-layer BGA package that is similar to the above-described three-layer embodiment, except that a BGA Vdd plane is also provided intermediate the BGA Vss plane and the traces on the lower surface of the BGA package. This embodiment is preferred because it may be fabricated from two pieces of symmetrical printed circuit board material, and because it reduces ground bounce for "0" to "1", as well as for "1" to "0" IC output signal transitions.

[0030] The BGA Vdd plane provides a plane that is relatively closer to the IC than is the underlying PCB Vdd plane, and reduces series inductance when the IC sources current, as in a "0" to "1" output signal transition. This "0" to "1" ground bounce improvement is in addition to the "1" to "0" current sinking improvement afforded by the BGA Vss plane, which also improves heat sinking.

[0031] Because it provides an even number of planes, the four-layer embodiment is preferred for ease of fabrication. This embodiment may be manufactured using two pieces of symmetrical double clad PCB material, wherein the clad on each piece of material provides two planes. As such, this embodiment provides technical advantages in ease and economy of fabrication over a three layer embodiment.

[0032] Further, when compared to a prior art two-layer BGA package, a four-layer embodiment according to the present invention reduces series inductance by about 50%, reduces the effective output impedance from about 250 Ω to about 50 Ω, and increases shunt capacitance to about 1.3 pF. When compared to a prior art two-layer BGA package, the four-layer embodiment reduces time delay through the packaged IC by about 2 ns, and improves thermal dissipation by about 50%.

[0033] Other features and advantages of the invention will appear from the following description in which the preferred embodiments have been set forth in detail, in conjunction with the accompanying drawings.

FIGURE 1 is a sectional view of a conventional two-layer ball grid array configuration for packaging an integrated circuit, according to the prior art;

FIGURE 2 is a sectional view of a three-layer ball grid array configuration for packaging an integrated circuit, according to the present invention;

FIGURE 3 is a sectional view of a four-layer ball grid array configuration for packaging an integrated circuit, according to the present invention;

FIGURE 4 is a computer simulation comparing voltage waveforms for the four-layer embodiment of Figure 3 and the two-layer embodiment for Figure 1, for a CMOS buffer integrated circuit.

[0034] In a first three-layer embodiment shown in Figure 2, the present invention provides a BGA package 50 with a BGA Vss plane 60 disposed between the upper and lower BGA package traces 8A, 8B, 8C, 8C', and 10A, 10B, 10C, 10C'. Among these BGA package traces, the present invention adds upper and lower BGA package Vss traces 8C', 10C' on the outer periphery of the BGA package. This embodiment is three-layered in that there are traces 8A, 8B, 8C, 8C' at the upper surface of the BGA package, there is an intermediate BGA Vss plane 60, and there are traces 10A, 10B, 10C, 10C' at the lower surface of the BGA package.

[0035] The embodiment of Figure 2 improves thermal dissipation performance and partially improves electrical performance in a BGA package when compared to

the two-layer embodiment of Figure 1. These improvements result by providing a BGA Vss plane 60 relatively close to IC die 12, and by optionally providing outer Vss planes 8C', 10C' (and associated vias 6C' and outer solder balls 14C'). Outer planes or traces 8C', 10C' may be donut-shaped, and are coupled together by the BGA Vss plane 60, to which planes or traces 8C, 10C are also coupled. This coupling is affected by the vias 6C, 6C' which pass tightly through via-sized openings in plane 60 such that electrical (and thermal) contact results. By contrast, all other vias (e.g., 6A, 6B) pass through oversized openings in plane 60 that are sufficiently large as to not make electrical (or thermal) contact with the Vss plane 60.

[0036] As was the case in Figure 1, an IC die 12 mounted within the BGA package has its substrate coupled to a BGA package IC die Vss trace or plane 8C on the upper surface of the BGA package. A plurality of vias 6C, 6C' electrically and thermally couple the BGA Vss plane 60 to the BGA package IC die Vss trace 8C, and to the outer periphery traces 8C', 10C' on the upper and lower BGA package surfaces. Vss solder balls couple the various Vss traces on the lower BGA package surface to corresponding Vss planes on an underlying system PCB. As in the prior art, Vdd solder balls couple the various Vdd and signal traces on the lower BGA package surface to corresponding traces and planes on the underlying system PCB. Vdd vias 6A and signal vias 6B also couple respective Vdd and signal traces 8A, 14A and 8B, 14B.

[0037] It is understood that the BGA Vss plane 60 makes electrical contact with the Vss vias 6C, 6C', but not with the Vdd vias 6A or the signal vias 6B. Electrical connection with vias 6A, 6B is avoided by defining through openings in the BGA Vss plane 60 sufficiently large to permit vias 6A, 6B to pass through without contact between the outer wall of the via and the inner surface of the opening in plane 60. By contrast, the Vss vias 6C, 6C' pass through openings defined in plane 60 that will result in electrical contact.

[0038] The additional BGA Vss plane preferably is a copper clad surface on a portion of PCB material from which the BGA package is fabricated. In Figure 2, BGA Vss plane may be either the lower copper clad on a piece of symmetrical printed circuit board material 52 whose core is shown as 56, or the upper copper clad on a piece of symmetrical printed circuit board material 54 whose core is shown as 58. Typically, core 56 and core 58 will typically have a combined thickness of at least 0.02" to 0.03" (0.5 mm to 0.8 mm) to provide rigidity for BGA package 50. In practice, core 56 may be relatively thin (e.g., 0.005" or 0.13 mm) material to place BGA Vss plane 60 closer to IC 12. If desired, the thickness of core 58 may be increased to compensate for a thinner core 56, to maintain overall rigidity for BGA package 50.

[0039] Thermally, heat from IC 12 is coupled from the BGA package IC die Vss trace 12 through vial 6C to the BGA Vss plane 60, through the lower portion of the same vias to the BGA package Vss trace 14C on the lower surface of BGA package 50. From trace 14C, conduction to the Vss plane 20C on the system PCB 18 occurs (after soldering of BGA package 50 to the system PCB 18). The BGA Vss plane 60 may be relatively closer to the IC than is the underlying system PCB 18, and will thus sink heat and allow IC 12 to operate at a lower package temperature. A three-layer BGA package as depicted in Figure 2 will exhibit a θ_{ja} of about 20°C/W.

[0040] Electrically, the BGA Vss plane 60 provides a closer and lower impedance Vss plane for sinking current output by IC 12 than is provided by the underlying PCB Vss plane 20C. The closer proximity of this Vss plane to IC 12 actually increases slightly the shunt capacitance by perhaps 0.1 pF. In practice, this slight capacitance increase can help IC 12 performance by emulating a small decoupling capacitor that is moved closer to the IC. Although on IC signal output pads further shunt capacitance is undesired, the relative increase is small, e.g., from about 1.2 pF to about 1.3 pF.

[0041] As shown in Figure 2, the upper surface of BGA package 50 provides both a. central BGA package IC die Vss trace 8C, and peripheral BGA package traces 8C'. As noted, these traces 8C, 8C' are coupled through vias 6C, 6C' to the BGA Vss plane 60 to corresponding traces 10C, 10C' on the lower surface of the BGA package, and thence through solder balls 14C, 14C' to corresponding traces 20C, 20C' on the system PCB 18.

[0042] So coupled, BGA Vss plane 60 advantageously reduces series inductance to IC 12, thus reducing ground bounce, at least for IC output signals transitioning from "1" to "0". The outer periphery BGA package traces 8C', 10C' and their associated vias and solder balls help maintain a low impedance between IC 12 and the BGA Vss plane 60, and thus help ensure that return current is present in the BGA Vss plane. If the outer BGA package Vss traces 8C', 14C' and associated vias and solder balls were eliminated, the ground bounce improvement otherwise available from BGA package 50 would suffer degradation, perhaps in the 40% range.

[0043] During a "1" to "0" IC output signal transition, a low impedance ground current return path is present in BGA Vss plane 60, since the effective series inductance L is minimized. As a result, IC 12 is not forced to provide a substantial current return path, and any $dV = Ldi/dt$ voltage changes at the Vss pad within IC 12 are relatively minimal during "1" to "0" output voltage transitions. In this fashion, the Vss pad within IC 12 can maintain a relatively stable potential with minimum voltage bounce, at least during DC and "1" to "0" output voltage conditions, with attendant current sinking.

[0044] Although the embodiment of Figure 2 provides improved thermal and electrical performance when compared to the prior art configuration of Figure 1, a three-layered embodiment is difficult to fabricate economically. As noted, BGA Vss plane may be either the lower surface of a PCB 52, or the upper surface of a PCB 54. As such, one of PCB 52 and 54 must be single

sided, which is to say a non-symmetrical PCB. Combining a generic double-sided PCB with a single-sided PCB using, for example, pre-preg material is expensive, time consuming, and simply not a preferred mode of construction. Similarly, coating a copper clad surface on a symmetrical PCB (e.g., 52) with a pre-preg material (e.g. 58) that is then clad with copper (e.g., layer 10) is likewise not a preferred mode of construction. Further, the three-layered embodiment of Figure 2 minimizes ground bounce during IC current sourcing transitions only, and does not improve ground bounce for IC current sinking transitions.

[0045] Figure 3 depicts a more preferred embodiment of the present invention, wherein a four-layer BGA package 100 is provided. This embodiment is somewhat similar to the above-described three-layer embodiment, except that a BGA Vdd plane 260 is also provided intermediate a BGA Vss plane 200 and the traces on the lower surface of the BGA package. This embodiment is preferred because it reduces ground bounce for "0" to "1" and for "1" to "0" IC output transitions. Further, this embodiment exhibits improved heat dissipation and advantageously may be fabricated from two pieces of symmetrical printed circuit board material.

[0046] Thermally, the four-layer embodiment of Figure 3 has a θ_{ja} of about 15°C/W, which compares very favorably to the 35°C/W rating of a prior art two layer embodiment. For a given dissipation, IC 12 packaged in the four-layer embodiment of Figure 3 can safely dissipate about twice as much heat as can the same IC in a prior art two-layer BGA package. Thus, while the two-layer packaged IC would require the additional expense and volume associated with heat sinking, heat sinking may be avoided by using the four-layer package described herein.

[0047] More specifically, as shown in Figure 3, a four-layer BGA package 100 provides a BGA Vss plane 200 and a BGA Vdd plane 260 disposed intermediate upper and lower BGA package conductive traces 8A, 8B, 8C, 8C', and 10A, 10B, 10C and 10C'. As in the embodiment of Figure 2, at least a portion of these upper and lower BGA package traces or places are in vertical registration to permit coupling therebetween using one or more vias.

[0048] Because it is generally more important to reduce bounce at an IC Vss pad than at the IC Vdd pad due to decreased "0" level noise margins, the BGA Vss plane 200 preferably is placed closer to IC 12 than is the BGA Vdd plane 260. Similar to what was described with respect to Figure 2, the addition of the BGA Vss plane decreases series inductance substantially, but increases slightly the shunt capacitance as seen by a signal pad on the IC. However, the approximately 0.1 pF increase (e.g., from 1.2 pF without the BGA Vss plane to about 1.3 pF) appears beneficial in decoupling the IC signal lines from noise.

[0049] In Figure 3, the Vss vias 6C, 6C' make electrical and thermal connection with the BGA Vss plane 200, but not with the underlying BGA Vdd plane 260. Similarly, the Vdd vias 6A are electrically insulated from the BGA Vss plane 200, but make electrical contact with the BGA Vdd plane 260. The various signal vias 6B are electrically insulated from both planes 200, 260. Such insulation can result from defining a relatively large opening in plane 200 and/or 260 through which a via passes that is not to make electrical contact with the plane.

[0050] As in the three-layer embodiment, vias 6A, 6B, 6C, 6C' connect corresponding upper and lower BGA package traces 8A, 8B, 8C, 8C' and 10A, 10B, 10C, 10C', with vias 6C thermally conducting heat from the die Vss plane 8C to the BGA Vss plane 200, and thence downward. As described with respect to Figure 2, solder balls 14A, 14B, 14C, 14C' provide electrical contact with corresponding traces 20A, 20B, 20C, 20C' on an underlying system PCB 18.

[0051] While vias 6C may also thermally conduct heat to the BGA Vdd plane 260 and the underlying system PCB ground plane or trace 20C, the Vdd plane 260 serves a relatively minor role in heat dissipation. More importantly, BGA Vdd plane 260 advantageously provides a Vdd plane that is relatively closer to IC 12 than is the underlying PCB Vdd plane or trace 20A. As a result, series inductance to IC 12 is reduced when the IC sources current, as in a "0" to "1" output signal transition. Further, as noted, the BGA Vss plane 200 reduces series inductance when IC 12 sinks current, as in a "1" to "0" output signal transition.

[0052] The four-layer embodiment is preferred for ease of fabrication in that it can be manufactured using two pieces of symmetrical double clad PCB material 270, 280 with a core 290 therebetween. As such, PCB 270 has a core 272 sandwiched between copper clad layers defining the BGA package upper traces 8A, 8B, 8C, 8C' and the BGA Vss plane 200. PCB 280 has a core 282 sandwiched between copper clad layers defining the BGA Vdd plane 260 and the BGA package lower traces 10A, 10B, 10C, 10C'. Cores 272 and 282 may advantageously be conventional 0.005" (0.13 mm) FR4 epoxy glass material, joined together by a pre-preg core 290 whose thickness is whatever is desired to provide necessary rigidity for the BGA package 100, e.g., 0.020" to 0.060" (0.5 mm to 1.5 mm).

[0053] Compared to a prior art two-layer BGA package, the four-layer embodiment of Figure 3 can reduce series inductance to about 6 nh to about 9 nh, and can reduce the effective IC output impedance to about 50 Ω. A 50 Ω output impedance advantageously permits high frequency signals from IC 12 to match 50 Ω transmission lines formed on the system PCB 18.

[0054] Figure 4 depicts a computer simulation showing the response of an IC buffer encapsulated in a four-layer BGA package as shown in Figure 3, as contrasted with the same buffer packaged in the prior art two-layer configuration of Figure 1. In each simulation, a positive-going pulse (V_{IN}) was provided as input, and a relatively heavy 50 pF load was assumed. V_{OUT4} represents the voltage output of the four-layer configuration of Figure

3, and V_{OUT2} represents the voltage output of the two-layer prior art configuration of Figure 1. Because of the heavy capacitive load, neither output voltage waveform exhibits ringing. However, the decreased series inductance associated with the four-layer embodiment is apparent by the approximately 2 ns decrease in delay as contrasted with the delay in V_{OUT2}. At the top and bottom of Figure 4, V_{dd4}, V_{dd2}, V_{ss4} and V_{ss2} depict the upper and lower power supply signals as seen at the IC. In each instance, supply voltages at the IC associated with the four-layer embodiment are cleaner and exhibit less bounce than the corresponding two-layer embodiment signals.

[0055] The improved voltage waveforms shown in Figure 4 result from diminished ground bounce in the four-layer package due to decreased effective series inductance. It will be appreciated that in a digital system comprising perhaps thousands of digital ICs that overall system reliability is enhanced by providing a four-layer BGA package according to the present invention. A more predictable noise margin is attained, and a more stable performance is realized, especially under increased ambient temperature, wherein the present invention advantageously permits the encapsulated IC to operate at lower junction temperature without heat sinking.

Claims

1. A ball grid array package (50) for an integrated circuit ("IC") (12), comprising:

upper layer package traces (8A-8C') which are suitable to be coupled to a corresponding IC pad by means of bond wires (22, 24),
lower layer package traces (10A-10C') with regions that are solderable to solder balls (14) used to solder said package (50) to an underlying system printed circuit board ("PCB") (18), the upper and lower layer traces (8A-8C'; 10A-10C') each including a Vss trace (8C, 10C), a Vdd trace (8A, 10A), and a signal trace (8B, 10B);
isolating material disposed between the upper and lower layer package traces (8A-8C'; 10A-10C') and comprising two cores (56, 58) having a combined thickness to provide rigidity to the package (50);
vias (6A-6C') including a Vdd via (6A) coupling the upper layer Vdd trace (8A) to a corresponding lower layer Vdd trace (10A) and a signal via (6B) coupling the upper layer signal trace (8B) to a corresponding lower layer signal trace (10B);
a Vss plane (60) disposed intermediate said upper and said lower layer package traces (8A-8C'; 10A-10C') and making contact with a Vss via (6C) coupled to an upper and lower layer Vss trace (8C, 10C);

characterized in that

one of said cores (56, 58) together with the Vss plane (60) and the package traces (8A-8C'; 10A-10C') belonging to this core forming a symmetrical PCB and the other core (58, 56) together with the package traces (8A-8C'; 10A-10C') belonging to said other core forming an asymmetrical PCB;

the vias (6A-6C') including the Vss via (6C) are unitary-construction vias extending through vertically aligned associated openings in the cores (56, 58) and the Vss plane (60) and thus through the combined thickness of said cores (56, 58) from the upper layer package traces (8A-8C') through cores (56, 58) to the lower layer package traces (10A-10C'); and

the lower layer package traces (10A-10C') coupled to corresponding ones of the upper layer package traces (8A-8C') through the vias (6A-6C') are in vertical alignment.

2. The package according to claim 1, **characterized by**

a third core (290) sandwiched between the Vss plane (200) of a first (272) of said two cores and a Vdd plane (260) of a second (282) of said two cores;

the three cores (260, 272, 282) and the Vss and Vdd Planes (200, 260) each having at least three via openings defined therethrough;

the Vdd via (6A) coupling the upper layer Vdd trace (8A) to the Vdd plane (260) and to the lower layer Vdd trace (10A) by passing through the via opening in the Vdd plane (260) while contacting the Vdd plane (260) and by passing through the via opening in the Vss plane (200) without contacting the Vss plane (200);

the signal via (6B) coupling the upper layer signal trace (8B) to the lower layer signal trace (10B) while passing through via openings in the Vss and Vdd planes (200, 260) without contacting the Vss or the Vdd planes (200, 260); and by

the Vss via (6C) coupling the upper layer. Vss trace (8C) to the Vss plane (200) and to the lower layer Vss trace (10C) by passing through the via opening in the Vss plane (200) while contacting the Vss plane (200) and by passing through the via opening in the Vdd plane, (260) without contacting the Vdd plane (260).

3. The package according to one of the claims 1 or 2, **characterized in that** said upper layer package Vss trace (8C) includes an IC die plane soldered to a substrate of said IC (12).

4. The package according to claim 2, **characterized**

in that at least one of said first core (272) and said second core (282) comprises a symmetrical PCB (170, 280).

5. The package according to claim 3 or 4, **characterized in that** said Vss plane (200) is disposed closer to said IC (12) than is said Vdd plane (260).

6. The package according to one of the claims 1 to 5, **characterized in that** said Vss plane (60, 200) is vertically spaced-apart from said substrate of said IC (12) at a distance less than 0.03" (0.8 mm).

7. The package according to one of the claims 1 to 6, **characterized in that** at least one core (56, 58, 272, 282, 290) includes a material selected from the group consisting of (a) FR4 epoxy glass, and (b) pre-preg.

8. The package according to one of the claims 1 to 7, **characterized by** an overmold (16) encapsulating said IC (12).

9. The package according to one of the claims 1 to 8, **characterized in that** the output impedance between a signal output pad on said IC (12) and said Vss plane (60, 200) is about 50 Ω.

10. The package according to one of the claims 1 to 9, **characterized in that** said IC (12) includes a digital circuit operating at a frequency of at least 30 MHz.

11. The package according to claim 1, **characterized in that** the upper layer Vdd and Vss traces (8A, 8C) are an upper layer surface Vdd and Vss plane, respectively, and **in that** the lower layer Vdd and Vss traces (10A, 10C) are a lower layer surface Vdd and Vss plane, respectively.

12. The package according to claim 11, **characterized in that** the output impedance between a signal output pad on said IC (12) and said upper layer surface Vss plane and said lower layer surface Vss plane is about 50 Ω.

13. A method of reducing ground bounce and increasing thermal dissipation in a ball grid array package (50) for an integrated circuit ("IC") (12), the package (50) comprising two cores (56, 58) sandwiched between upper and lower layer package traces (8A-8C'; 10A-10C') coupled together by vias (6A-6C'), said IC (12) suitable to be coupled to chosen ones of said upper layer package traces (8A-8C') by means of bond wires, and chosen ones of said lower layer package traces (10A-10C') being solderable to solder balls (14) adapted to be soldered to traces on an underlying system printed circuit board (18), the method comprising the following steps:

(a) disposing a Vss plane (60) intermediate said upper and lower layer package traces (8A-8C'; 10A-10C');
(b) coupling said Vss plane (60) using at least one Vss via (6C) to a Vss trace included among said upper and lower package traces (8A-8C'; 10A-10C');
(c) coupling an upper layer V_{DD} trace (8A) to a corresponding lower layer V_{DD} trace (10A) using at least one V_{DD} via (6A);
(d) coupling an upper layer signal trace (8B) to corresponding lower layer signal trace (10B) using at least one signal via (6B);
characterized by
(e) using a symmetrical printed circuit board for forming one of said cores (56, 58) together with the Vss plane (60) and the package traces (8A-8C'; 10A-10C') belonging to this core;
(f) using an asymmetrical printed circuit board for forming the other core (58, 56) together with the package traces (8A-8C'; 10A-10C') belonging to said other core;
(g) using as the vias (6A-6C') including the Vss via (6C) unitary-construction vias extending through vertically aligned associated openings in the cores (56, 58) and the Vss plane (60) and thus through the combined thickness of said cores (56, 58) from the upper layer package traces (8A-8C') through cores (56, 58) to the lower layer package traces (10A-10C'); and
(h) aligning the lower layer package traces (10A-10A') coupled to corresponding ones of the upper layer package traces (8A-8A') through the vias (6A-6C') in vertical direction.

14. The method according to claim 13, **characterized by**

disposing a V_{dd} plane (260) intermediate said Vss plane (200) and said lower package traces (10A-10C'); and

coupling said V_{dd} plane (260) using at least one V_{DD} via (6A) to a V_{dd} trace (8A) among said upper and lower package traces (8A-8C'; 10A-10C'), said V_{dd} plane (260) defining via openings through which other of said vias (6A-6C') not coupled to V_{dd} pass without making electrical contact.

15. The method according to claim 13 or 14, **characterized in that** for at least one of said (i) upper layer package traces (8A-8C'), a portion of said cores (56, 58, 272, 282), and said Vss plane (60, 200), and (ii) said V_{dd} plane (260), a portion of said cores (56, 58, 272, 282), and said lower layer package traces (10A-10C') double-sided printed symmetrical PCB material is chosen.

16. The method according to the claims 13 to 15, **characterized in that** a material comprised in said cores

(56, 58, 272, 282) is selected from the group consisting of (a) FR4 epoxy glass, and (b) pre-preg.

17. The method according to one of the claims 13 to 16, **characterized in that** at step (a) said Vss plane (60) is disposed vertically spaced apart from a substrate of said IC (12) at a distance less than 0.03" (0.8 mm).

Patentansprüche

1. Ball-Grid-Array-Gehäuse (50) für eine integrierte Schaltung ("IC") (12), das umfaßt:

Gehäusebahnen (8A-8C') einer oberen Schicht, die mit einem entsprechenden IC-Anschlußfleck über Bonddrähte (22, 24) gekoppelt werden können,
Gehäusebahnen (10A-10C') einer unteren Schicht mit verlötbaren Bereichen, um Kugeln (14), die zum Verlöten des Gehäuses (50) verwendet werden, mit einer darunterliegenden gedruckten System-Leiterplatte (System-"PCB") (18) zu verlöten,
wobei die Bahnen der oberen und unteren Schichten (8A-8C'; 10A-10C') jeweils eine Vss-Bahn (8C, 10C), eine Vdd-Bahn (8A, 10A) und eine Signalbahn (8B, 10B) enthalten;
Isoliermaterial, das zwischen den Gehäusebahnen (8A-8C'; 10A-10C') der oberen und unteren Schichten angeordnet ist und zwei Kerne (56, 58) umfaßt, die eine kombinierte Dicke besitzen, um für das Gehäuse (50) eine Starrheit zu schaffen;
Durchgangslöcher (6A-6C'), die ein Vdd-Durchgangsloch (6A), das die Vdd-Bahn (8A) der oberen Schicht mit einer entsprechenden Vdd-Bahn (10A) der unteren Schicht koppelt, und ein Signaldurchgangsloch (6B), das die Signalbahn (8B) der oberen Schicht mit einer entsprechenden Signalbahn (10B) der unteren Schicht koppelt, umfassen;
eine Vss-Ebene (60), die zwischen den Gehäusebahnen (8A-8C'; 10A-10C') der oberen und unteren Schichten angeordnet ist und einen Kontakt mit einem Vss-Durchgangsloch (6C) herstellt, das mit einer Vss-Bahn (8C, 10C) der oberen und unteren Schichten gekoppelt ist;

dadurch gekennzeichnet, daß

einer der Kerne (56, 58) zusammen mit der Vss-Ebene (60) und den Gehäusebahnen (8A-8C'; 10A-10C'), die zu diesem Kern gehören, eine symmetrische PCB bilden und der andere Kern (58, 56) zusammen mit den Gehäusebahnen (8A-8C'; 10A-10C'), die zu dem anderen Kern gehören, eine asymmetrische PCB bilden;

die Durchgangslöcher (6A-6C'), die das Vss-Durchgangsloch (6C) enthalten, Durchgangslöcher mit einheitlicher Konstruktion sind, die sich durch vertikal ausgerichtete zugeordnete Öffnungen in den Kernen (56, 58) und der Vss-Ebene (60) und somit durch die kombinierte Dicke der Kerne (56, 58) von den Gehäusebahnen (8A-8C') der oberen Schicht durch die Kerne (56, 58) zu den Gehäusebahnen (10A-10C') der unteren Schicht erstrecken; und

die Gehäusebahnen (10A-10C') der unteren Schicht, die mit entsprechenden der Gehäusebahnen (8A-8C') der oberen Schicht durch die Durchgangslöcher (6A-6C') gekoppelt sind, vertikal ausgerichtet sind.

2. Gehäuse nach Anspruch 1, **gekennzeichnet durch**

einen dritten Kern (280), der zwischen der Vss-Ebene (200) eines ersten (272) der zwei Kerne und einer Vdd-Ebene (260) eines zweiten (282) der zwei Kerne sandwichartig angeordnet ist;

wobei die drei Kerne (260, 272, 282) und die Vss- und Vdd-Ebenen (200, 260) jeweils wenigstens drei Durchgangslochöffnungen besitzen, die durch sie hindurch definiert sind;

wobei das Vdd-Durchgangsloch (6A) die Vdd-Bahn (8A) der oberen Schicht mit der Vdd-Ebene (260) und mit der Vdd-Bahn (10A) der unteren Schicht koppelt, indem es durch die Durchgangsöffnung in der Vdd-Ebene (260) verläuft und dabei mit der Vdd-Ebene (260) einen Kontakt herstellt und indem es durch die Durchgangsöffnung in der Vss-Ebene (200) verläuft, ohne mit der Vss-Ebene (200) einen Kontakt herzustellen;

wobei das Signaldurchgangsloch (6B) die Signalbahn (8B) der oberen Schicht mit der Signalbahn (10B) der unteren Schicht koppelt und dabei durch Durchgangsöffnungen in den Vss- und Vdd-Ebenen (200, 260) verläuft, ohne einen Kontakt mit den Vss- oder Vdd-Ebenen (200, 260) herzustellen; und

wobei das Vss-Durchgangsloch (6C) die Vss-Bahn (8C) der oberen Schicht mit der Vss-Ebene (200) und mit der Vss-Bahn (10C) der unteren Schicht koppelt, indem es durch die Durchgangsöffnung in der Vss-Ebene (200) verläuft und dabei einen Kontakt mit der Vss-Ebene (200) herstellt und indem es durch die Durchgangsöffnung in der Vdd-Ebene (260) verläuft, ohne einen Kontakt mit der Vdd-Ebene (260) herzustellen.

3. Gehäuse nach einem der Ansprüche 1 oder 2, **dadurch gekennzeichnet, daß** die Gehäuse-Vss-Bahn (8C) der oberen Schicht eine IC-Chipebene enthält, die mit einem Substrat des IC (12) verlötet ist.

4. Gehäuse nach Anspruch 2, **dadurch gekennzeichnet, daß** der erste Kern (272) und/oder der zweite Kern (282) eine symmetrische PCB (170, 280) enthält.

5. Gehäuse nach Anspruch 3 oder 4, **dadurch gekennzeichnet, daß** die Vss-Ebene (200) näher bei der IC (12) als die Vdd-Ebene (260) angeordnet ist.

6. Gehäuse nach einem der Ansprüche 1 bis 5, **dadurch gekennzeichnet, daß** die Vss-Ebene (60, 200) von dem Substrat der IC (12) um eine Strecke vertikal beabstandet ist, die kleiner als 0,03" (0,8 mm) ist.

7. Gehäuse nach einem der Ansprüche 1 bis 6, **dadurch gekennzeichnet, daß** wenigstens ein Kern (56, 58, 272, 282, 290) einen Werkstoff enthält, der aus der Gruppe gewählt ist, die aus (a) FR4-Epoxidglas und (b) Pre-Preg besteht.

8. Gehäuse nach einem der Ansprüche 1 bis 7, **gekennzeichnet durch** einen Überguß (16), der die IC (12) einkapselt.

9. Gehäuse nach einem der Ansprüche 1 bis 8, **dadurch gekennzeichnet, daß** die Ausgangsimpedanz zwischen einem Signalausgang-Anschlußfleck auf der IC (12) und der Vss-Ebene (60, 200) etwa 50 Ω beträgt.

10. Gehäuse nach einem der Ansprüche 1 bis 9, **dadurch gekennzeichnet, daß** die IC (12) eine digitale Schaltung enthält, die mit einer Frequenz von wenigstens 30 MHz arbeitet.

11. Gehäuse nach Anspruch 1, **dadurch gekennzeichnet, daß** die Vddund Vss-Bahnen (8A, 8C) der oberen Schicht eine Oberflächen-Vdd-Ebene bzw. eine Oberflächen-Vss-Ebene der oberen Schicht sind und daß die Vdd- und Vss-Bahnen (10A, 10C) der unteren Schicht eine Oberflächen-Vdd-Ebene bzw. eine Oberflächen-Vss-Ebene der unteren Schicht sind.

12. Gehäuse nach Anspruch 11, **dadurch gekennzeichnet, daß** die Ausgangsimpedanz zwischen einem Signalausgang-Anschlußfleck auf der IC (12) und der Oberflächen-Vss-Ebene der oberen Schicht und der Oberflächen-Vss-Ebene der unteren Schicht etwa 50 Ω beträgt.

13. Verfahren zum Verringern des Ground-Bounce und zum Erhöhen der Wärmeabführung in einem Ball-Grid-Array-Gehäuse (50) für eine integrierte Schaltung ("IC") (12), wobei das Gehäuse (50) zwei Kerne (56, 58) umfaßt, die zwischen Gehäusebahnen (8A-8C'; 10A-10C') oberer und unterer Schichten, die durch Durchgangslöcher (6A-6C') gekoppelt sind, sandwichartig angeordnet sind, wobei die IC (12) mit ausgewählten der Gehäusebahnen (8A-8C') der oberen Schicht mittels Bonddrähten und mit ausgewählten der Gehäusebahnen (10A-10C') der unteren Schicht, die mit Lötkugeln (14) verlötet werden können, die mit Bahnen auf einer darunterliegenden gedruckten System-Leiterplatte (18) verlötet werden können, gekoppelt werden kann, wobei das Verfahren die folgenden Schritte umfaßt:

(a) Anordnen einer Vss-Ebene (60) zwischen den Gehäusebahnen (8A-8C'; 10A-10C') der oberen und unteren Schichten;
(b) Koppeln der Vss-Ebene (60) unter Verwendung wenigstens eines Vss-Durchgangslochs (6C) mit einer Vss-Bahn, die in den oberen und unteren Gehäusebahnen (8A-8C'; 10A-10C') enthalten ist;
(c) Koppeln einer Vdd-Bahn (8A) der oberen Schicht mit einer entsprechenden Vdd-Bahn (10A) der unteren Schicht unter Verwendung wenigstens eines Vdd-Durchgangslochs (6A);
(d) Koppeln einer Signalbahn (8B) der oberen Schicht mit einer entsprechenden Signalbahn (10B) der unteren Schicht unter Verwendung wenigstens eines Signaldurchgangslochs (6B);
gekennzeichnet durch
(e) Verwenden einer symmetrischen gedruckten Leiterplatte für die Bildung eines der Kerne (56, 58) zusammen mit der Vss-Ebene (60) und den Gehäusebahnen (8A-8C'; 10A-10C'), die zu diesem Kern gehören;
(f) Verwenden einer asymmetrischen gedruckten Leiterplatte, um den anderen Kern (58, 56) zusammen mit den Gehäusebahnen (8A-8C'; 10A-10C'), die zu dem anderen Kern gehören, zu bilden;
(g) Verwenden von Durchgangslöchern mit einheitlicher Konstruktion für die Durchgangslöcher (6A-6C') einschließlich des Vss-Durchgangslochs (6C), die sich durch vertikal ausgerichtete zugeordnete Öffnungen in den Kernen (56, 58) und in der Vss-Ebene (60) und somit durch die kombinierte Dicke der Kerne (56, 58) von den Gehäusebahnen (8A-8C') der oberen Schicht durch Kerne (56, 58) zu den Gehäusebahnen (10A-10C') der unteren Schicht erstrecken; und
(h) Ausrichten der Gehäusebahnen (10A-10A') der unteren Schicht, die mit entsprechenden der Gehäusebahnen (8A-8A') der oberen Schicht durch die Durchgangslöcher (6A-6C') gekoppelt sind, auf die vertikale Richtung.

14. Verfahren nach Anspruch 13, **gekennzeichnet durch**

Anordnen einer Vdd-Ebene (260) zwischen der Vss-Ebene (200) und den unteren Gehäusebahnen (10A-10C'); und

Koppeln der Vdd-Ebene (260) unter Verwendung wenigstens eines Vdd-Durchgangslochs (6A) mit einer Vdd-Bahn (8A) der oberen und unteren Gehäusebahnen (8A-8C'; 10A-10C'), wobei die Vdd-Ebene (260) Durchgangsöffnungen definiert, durch die andere der Durchgangslöcher (6A-6C'), die nicht mit Vdd gekoppelt sind, verlaufen, ohne einen elektrischen Kontakt herzustellen.

15. Verfahren nach Anspruch 13 oder 14, **dadurch gekennzeichnet, daß** für die (i) Gehäusebahnen (8A-8C') der oberen Schicht, einen Teil der Kerne (56, 58, 272, 282) und die Vss-Ebene (60, 200) und/oder (ii) für die Vdd-Ebene (260), einen Teil der Kerne (56, 58, 272, 282) und die Gehäusebahnen (10A-10C) der unteren Schicht ein doppelseitig bedrucktes symmetrisches PCB-Material gewählt wird.

16. Verfahren nach den Ansprüchen 13 bis 15, **dadurch gekennzeichnet, daß** ein in den Kernen (56, 58, 272, 282) enthaltener Werkstoff aus der Gruppe gewählt ist, die aus (a) FR4-Epoxidglas und (b) Pre-Preg besteht.

17. Verfahren nach einem der Ansprüche 13 bis 16, **dadurch gekennzeichnet, daß** im Schritt (a) die Vss-Ebene (60) so angeordnet wird, daß sie von einem Substrat der IC (12) vertikal um eine Strecke beabstandet ist, die kleiner als 0,03" (0,08 mm) ist.

Revendications

1. Boîtier de conditionnement à réseau de billes (50) pour un circuit intégré ("IC") (12), comprenant:

des pistes de boîtier de couche supérieure (8A à 8C') qui sont agencées de manière à être couplées à un plot de circuit IC correspondant au moyen de fils de liaison (22, 24),
des pistes de boîtier de couche inférieure (10A à 10C') avec des zones qui peuvent être soudées sur des billes de soudure (14) utilisées pour souder ledit boîtier (50) sur une plaque de circuit imprimé ("PCB") de dispositif sous-jacente (18),
les pistes de couches supérieure et inférieure (8A à 8C' ; 10A à 10C') comprenant chacune une piste V_{ss} (8C, 10C), une piste V_{dd} (8A, 10A) et une piste de signal (8B, 10B) ;
un matériau isolant disposé entre les pistes de boîtier de couches supérieure et inférieure (8A à 8C', 10A à 10C') et comprenant deux noyaux (56, 58) présentant une épaisseur cumulée de manière à assurer une certaine rigidité au boîtier (50) ;
des voies de passage (6A à 6C') comprenant une voie de passage V_{dd} (6A) couplant la piste V_{dd} de couche supérieure (8A) à une piste V_{dd} de couche inférieure correspondante (10A) et une voie de passage de signal (6B) couplant la piste de signal de couche supérieure (8B) à une piste de signal de couche inférieure correspondante (10B) ;
un plan V_{ss} (60) disposé de manière intermédiaire par rapport à ladite piste de boîtier de couche supérieure et à ladite piste de boîtier de couche inférieure (8A, à 8C' ; 10A, à 10C') et assurant un contact avec une voie de passage V_{ss} (6C) couplée à une piste V_{ss} de couche supérieure et de couche inférieure (8C, 10C) ;

caractérisé en ce que:

l'un desdits noyaux (56, 58), ensemble avec le plan V_{ss} (60) et les pistes de boîtier (8A à 8C' ; 10A à 10C') appartenant à ce noyau, formant une plaque PCB symétrique et l'autre noyau (56, 56), ensemble avec les pistes de boîtier (8A à 8C', 10A à 10C') appartenant à cet autre noyau, formant une plaque PCB asymétrique ; les voies de passage (6A à 6C') comprenant la voie de passage V_{ss} (6C) sont des voies de passage de construction unitaire s'étendant à travers des ouvertures associées alignées verticalement dans les noyaux (56, 58) et le plan V_{ss} (60) et, ainsi, à travers l'épaisseur cumulée desdits noyaux (56, 58) à partir des pistes de boîtier de couche supérieure (8A à 8C') à travers les noyaux (56, 58) vers les pistes de boîtier de couche inférieure (10A à 10C') ; et
les pistes de boîtier de couche inférieure (10A à 10C') couplées à des pistes correspondantes des pistes de boîtier de couche supérieure (8A à 8C') à travers les voies de passage (6A à 6C') sont alignées verticalement.

2. Boîtier de conditionnement selon la revendication 1, **caractérisé par:**

un troisième noyau (290) intercalé entre le plan V_{ss} (200) d'un premier (272) desdits deux noyaux et un plan V_{dd} (260) d'un second (282) desdits deux noyaux ;
les trois noyaux (260, 272, 282) et les plans V_{ss} et V_{dd} (200, 260) comportant chacun au moins trois ouvertures de voie de passage les traversant :

la voie de passage V_{dd} (6A) couplant la piste V_{dd} de couche supérieure (8A) au plan V_{dd} (260) et à la piste V_{dd} de couche inférieure (10A) en passant à travers l'ouver-

ture de voie de passage dans le plan V_{dd} (260) tout assurant le contact avec le plan V_{dd} (260) et en passant à travers l'ouverture de voie de passage dans le plan V_{ss} (200) sans venir en contact avec le plan V_{ss} (200) ;
la voie de passage de signal (6B) couplant la piste de signal de couche supérieure (8B) à la piste de signal de couche inférieure (10B) tout en passant à travers des ouvertures de voie de passage dans les plans V_{ss} et V_{dd} (200, 260) sans venir en contact avec les plans V_{ss} ou V_{dd} (200, 260) ; et par
la voie de passage V_{ss} (6C) couplant la piste V_{ss} de couche supérieure (8C) au plan V_{ss} (200) et à la piste V_{ss} de couche inférieure (10C) en passant à travers l'ouverture de voie de passage dans le plan V_{ss} (200) tout en assurant le contact avec le plan V_{ss} (200) et en passant à travers l'ouverture de voie de passage dans le plan V_{dd} (260) sans venir en contact avec le plan V_{dd} (260).

3. Boîtier de conditionnement selon la revendication 1 ou 2, **caractérisé en ce que** ladite piste V_{ss} de boîtier de couche supérieure (8C) comprend un plan de pastille de circuit IC soudé sur un substrat dudit circuit IC (12).

4. Boîtier de conditionnement selon la revendication 2, **caractérisé en ce qu'**au moins l'un desdits premier noyau (272) et second noyau (282) comprend une plaque PCB symétrique (170, 280).

5. Boîtier de conditionnement selon la revendication 3 ou 4, **caractérisé en ce que** ledit plan V_{ss} (200) est disposé plus près dudit circuit IC (12) que ledit plan V_{dd} (260).

6. Boîtier de conditionnement selon l'une des revendications 1 à 5, **caractérisé en ce que** ledit plan V_{ss} (60, 200) est espacé verticalement par rapport audit substrat dudit circuit IC (12) à une distance inférieure à 0,8 mm (0,03").

7. Boîtier de conditionnement selon l'une des revendications 1 à 6, **caractérisé en ce qu'**au moins un noyau (56, 58, 272, 282, 290) comprend un matériau sélectionné à partir du groupe constitué par (a) du verre époxy FR4 et (b) un préimprégné.

8. Boîtier de conditionnement selon l'une des revendications 1 à 7, **caractérisé par** un surmoulage (16) enrobant ledit circuit IC (12).

9. Boîtier de conditionnement selon l'une des revendications 1 à 8, **caractérisé en ce que** l'impédance de sortie entre un plot de sortie de signal sur ledit circuit IC (12) et ledit plan V_{ss} (60, 200) est de 50 Ω environ.

10. Boîtier de conditionnement selon l'une des revendications 1 à 9, **caractérisé en ce que** ledit circuit IC (12) comprend un circuit numérique fonctionnant à une fréquence d'au moins 30 MHz.

11. Boîtier de conditionnement selon la revendication 1, **caractérisé en ce que** les pistes Vdd et V_{ss} de couche supérieure (8A, 8C) sont respectivement un plan V_{dd} et V_{ss} de surface de couche supérieure et, **en ce que** les pistes V_{dd} et V_{ss} de couche inférieure (10A, 10C) sont respectivement un plan V_{dd} et V_{ss} de surface de couche inférieure.

12. Boîtier de conditionnement selon la revendication 11, **caractérisé en ce que** l'impédance de sortie entre un plot de sortie de signal sur ledit circuit IC (12) et ledit plan V_{ss} de surface de couche supérieure et ledit plan V_{ss} de surface de couche inférieure est de 50 Ω environ.

13. Procédé de réduction du rebond de masse et d'augmentation de la dissipation thermique dans un boîtier de conditionnement à réseau de billes (50) pour un circuit intégré ("IC") (12), le boîtier de conditionnement (50) comprenant deux noyaux (56, 58) intercalés entre des pistes de boîtier de couches supérieure et inférieure (8A à 8C' ; 10A à 10C') couplées entre-elles par des voies de passage (6A à 6C'), ledit circuit IC (12) étant adapté de manière à être couplé à des pistes sélectionnées desdites pistes de boîtier de couche supérieure (8A à 8C') au moyen de fils de liaison, et des pistes sélectionnées desdites pistes de boîtier de couche inférieure (10A à 10C') pouvant être soudées sur des billes de soudure (14) agencées de manière à être soudées sur les pistes d'une plaque de circuit imprimé de dispositif sous-jacente (18), le procédé comprenant les étapes suivantes:

(a) d'agencement d'un plan V_{ss} (60) de manière intermédiaire par rapport auxdites pistes de boîtier de couches supérieure et inférieure (8A à 8C' ; 10A à 10C');
(b) de couplage dudit plan V_{ss} (60), en utilisant au moins une voie de passage V_{ss} (6C), à une piste V_{ss} contenue dans lesdites pistes de boîtier de conditionnement supérieure et inférieure (8A à 8C' ; 10A à 10C') ;
(c) de couplage d'une piste V_{dd} de couche supérieure (8A) à une piste V_{dd} de couche inférieure (10A) correspondante en utilisant au moins une voie de passage Vdd (6A) ;
(d) de couplage d'une piste de signal de couche

supérieure (8B) à une piste de signal de couche inférieure correspondante (10B) en utilisant au moins une voie de passage de signal (68) ;

caractérisé par

(e) l'utilisation d'une plaque de circuit imprimé symétrique afin de former un premier desdits noyaux (56, 58) ensemble avec le plan V_{ss} (60) et les pistes de boîtier (8A à 8C' ; 10A à 10C') appartenant à ce noyau ;

(f) l'utilisation d'une plaque de circuit imprimé asymétrique afin de former l'autre noyau (58, 56) ensemble avec les pistes de boîtier (8A à 8C' ; 10A à 10C') appartenant audit autre noyau ;

(g) l'utilisation, pour les voies de passage (6C, 6C') comprenant la voie de passage V_{ss} (6C), de voies de passage de construction unitaire s'étendant à travers des ouvertures associées alignées verticalement dans les noyaux (56, 58) et le plan V_{ss} (60) et, ainsi, à travers l'épaisseur cumulée desdits noyaux (56, 58) à partir des pistes de boîtier de couche supérieure (8A à 8C') à travers les noyaux (56, 58) vers les pistes de boîtier de couche inférieure (10A à 10C'); et

(h) l'alignement des pistes de boîtier de couche inférieure (10A à 10A') couplées aux pistes correspondantes des pistes de boîtier de couche supérieure (8A, 8A') à travers les voies de passage (6A, 6C') dans la direction verticale.

14. Procédé selon la revendication 13, **caractérisé par:**

l'agencement d'un plan V_{dd} (260) de manière intermédiaire par rapport audit plan V_{ss} (200) et auxdites pistes de boîtier inférieures (10A à 10C') ; et

le couplage dudit plan (V_{dd}) (260), en utilisant au moins une voie de passage V_{dd} (6A), à une piste V_{dd} (8A) desdites pistes de boîtier supérieures et inférieures (8A à 8C' ; 10A à 10C'), ledit plan V_{dd} (260) définissant des ouvertures de voie de passage à travers lesquelles d'autres desdites voies de passage (6A, 6C') non couplées à V_{dd} passent sans assurer de contact électrique.

15. Procédé selon la revendication 13 ou 14, **caractérisé en ce que** pour au moins l'une (i) desdites pistes de boîtier de couche supérieure (8A à 8C'), une partie desdits noyaux (56, 58, 272, 282) et dudit plan V_{ss} (60, 200), et (ii) ledit plan V_{dd} (260), une partie desdits noyaux (58, 58, 272, 282), et lesdites pistes de boîtier de couche inférieure (10A à 10C'), on choisit un matériau de plaque PCB symétrique imprimé en double face.

16. Procédé selon les revendications 13 à 15, **caractérisé en ce que** le matériau constituant lesdits noyaux (56, 58, 272, 282) est sélectionné à partir du groupe comprenant (a) un verre époxy FR4, et (b) un préimprégné.

17. Procédé selon l'une des revendications 13 à 16, **caractérisé en ce qu'**à l'étape (a), ledit plan V_{ss} (60) est disposé verticalement à distance d'un substrat dudit circuit intégré IC (12) d'une valeur inférieure à 0,8 mm (0.03").

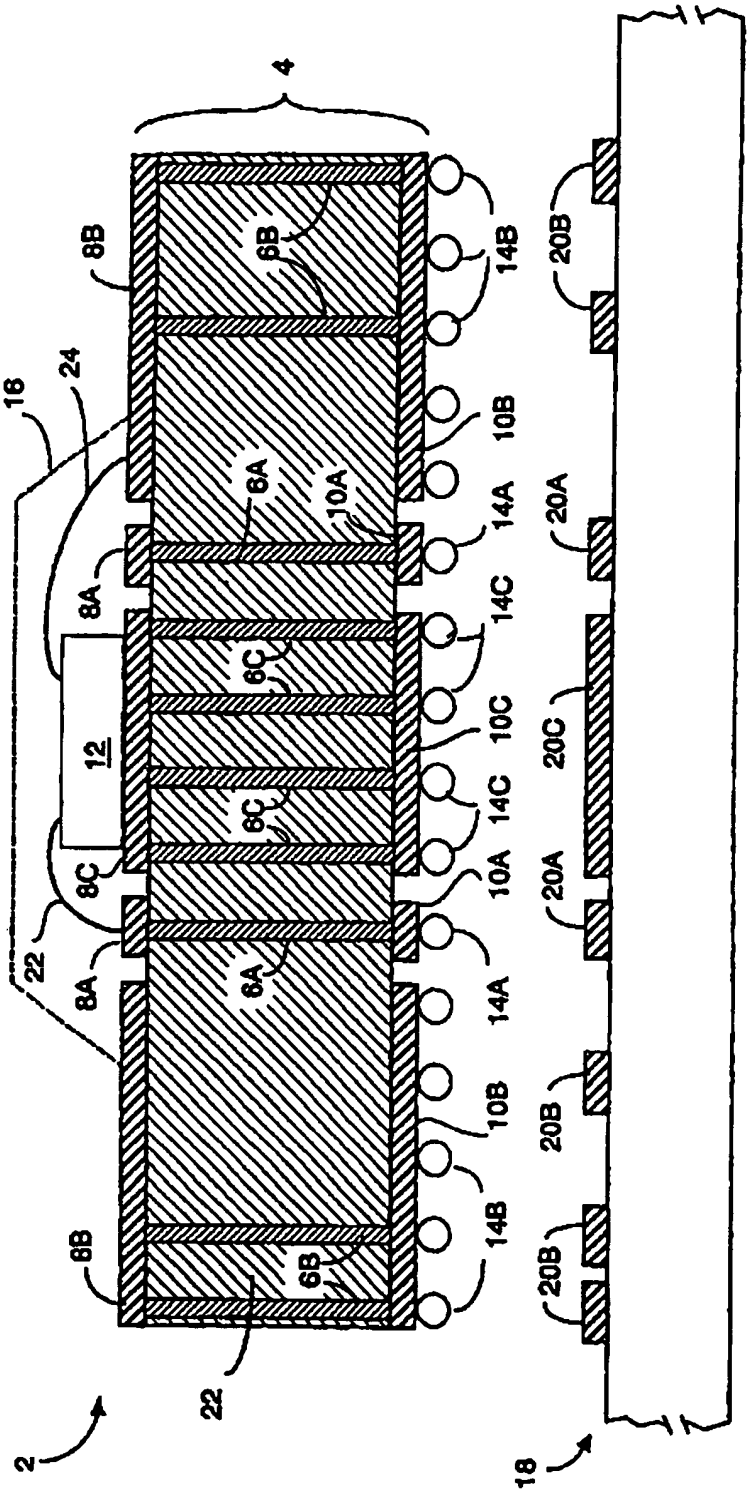

FIGURE 1
(PRIOR ART)

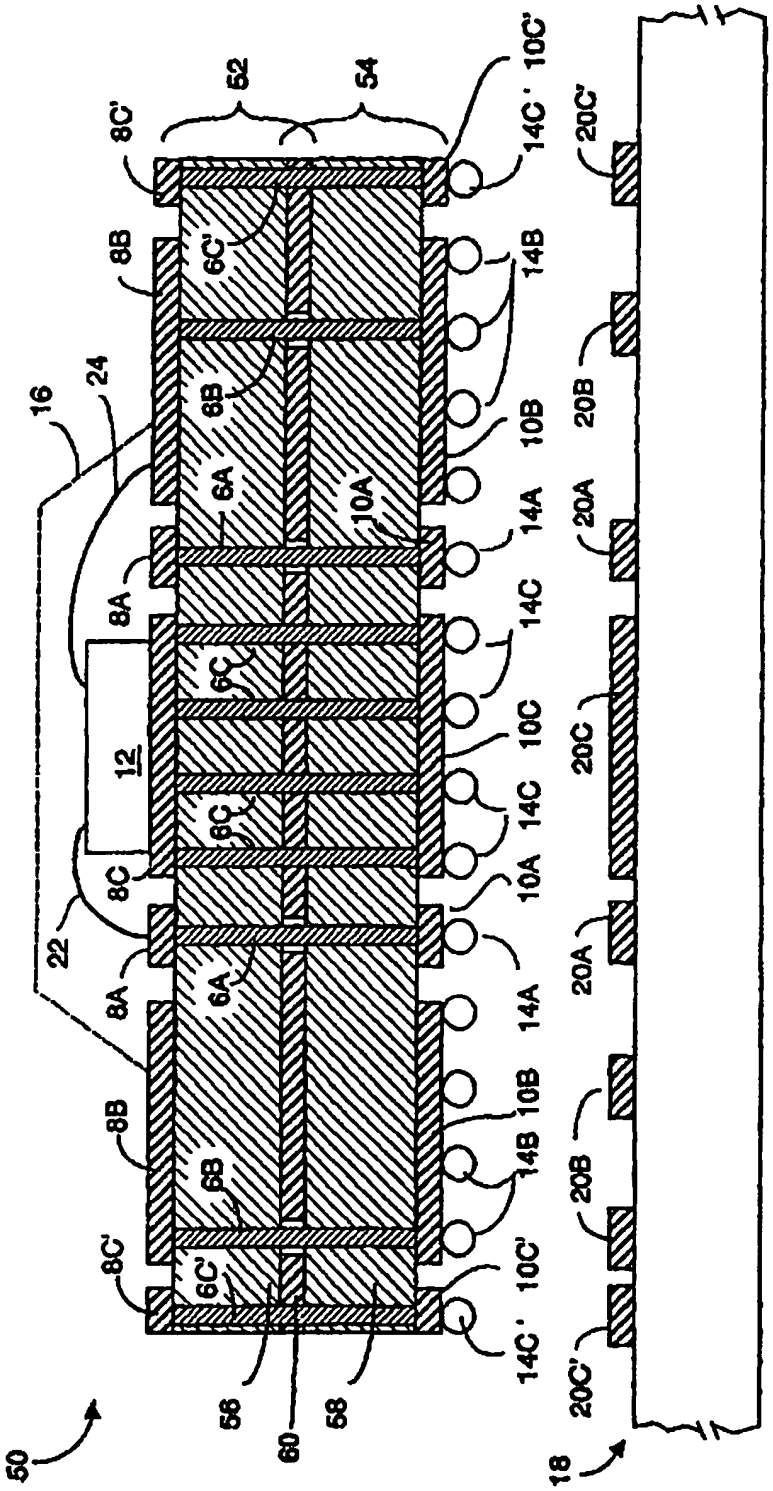
52
54
8C'
14C'
10C'
20C'
8B
6C'
14B
20B
16
24
6B
10B
6A
10A
14A
20A
8A
6C
14C
12
10C
20C
8C
22
50
56
60
58
18

FIGURE 2

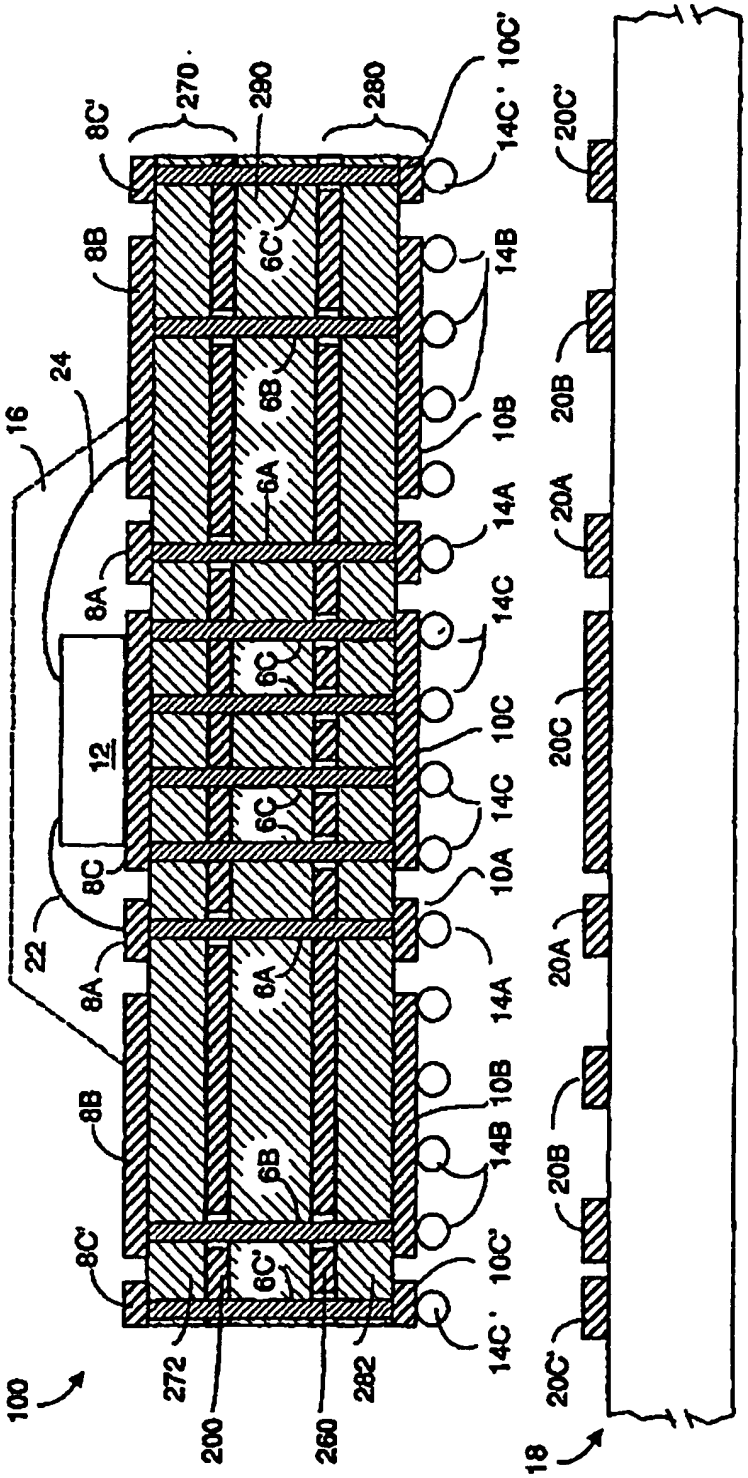
100
272
200
260
282
270
290
280
8C'
8B
8A
8C
6C'
6B
6A
6C
12
16
24
22
14C' 10C'
14B
10B
14A
14C
10C
10A
20C'
20B
20A
20C
18

FIGURE 3

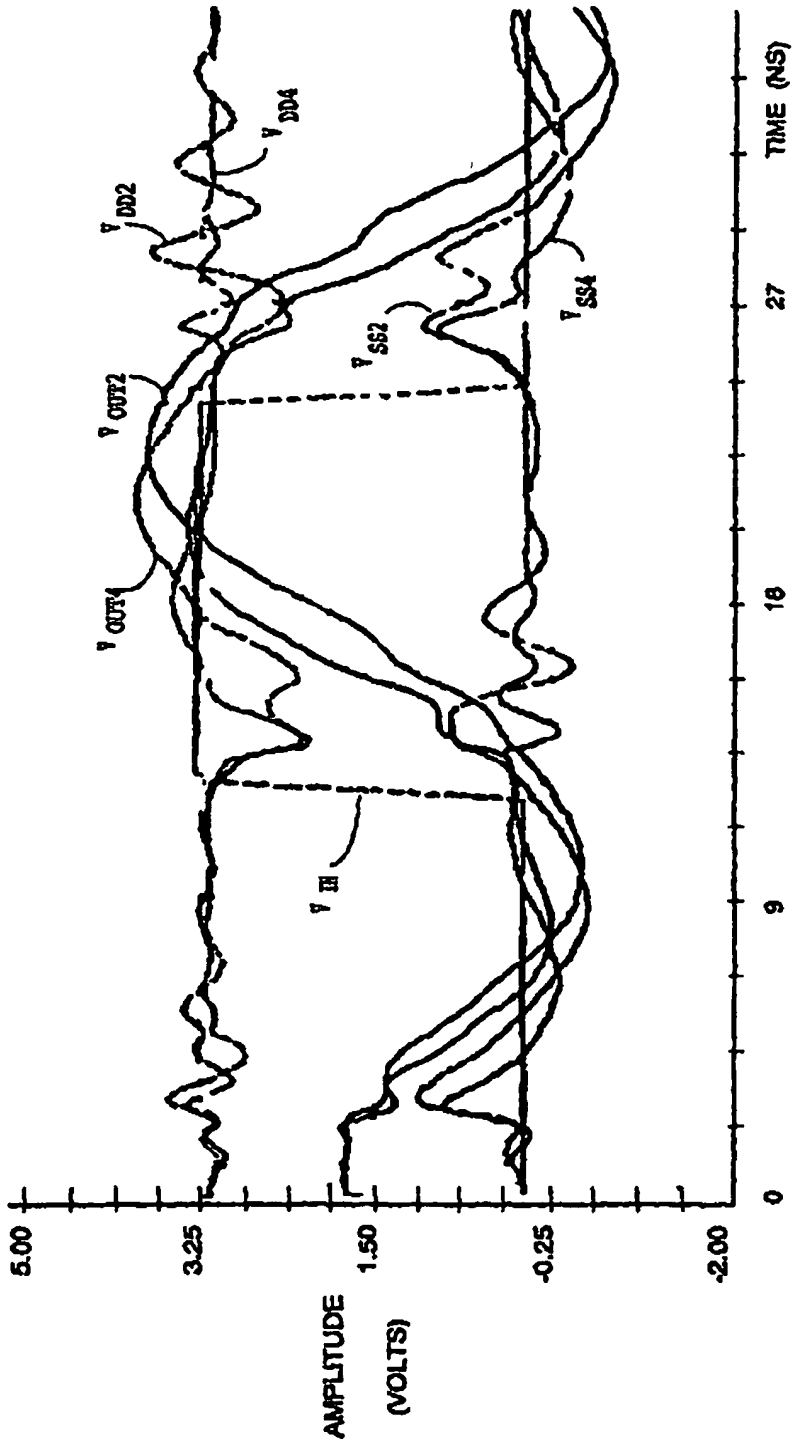
5.00
3.25
1.50
-0.25
-2.00
AMPLITUDE
(VOLTS)
0
9
18
27
TIME (NS)
V DD4
V DD2
V OUT2
V OUT1
V SS2
V SS4
V TH

FIGURE 4